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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/098,190 | 06/16/98 | SHEATS J | 10980239-1 |

| EXAMINER | |
|---|---|
| PIZIALI,J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2778 | 9 |

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IP ADMINISTRATION
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**DATE MAILED:** 01/03/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/098,190 | Sheats et al. |
| **Examiner** | **Group Art Unit** |
| Jeff Pizlali | 2778 |

☒ Responsive to communication(s) filed on *Jun 16, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claim**

☒ Claim(s) *1-12* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-12* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

**Application Papers**

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Jun 16, 1998* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

***— SEE OFFICE ACTION ON THE FOLLOWING PAGES —***

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference signs not mentioned in the description: Figure 1's 24, 34 and 36. Correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Dingwall (5,903,246).

In regards to claim 1, Dingwall discloses a display [column 2, lines 5-9] comprising a plurality of light emitting pixels (P), each pixel (P) comprising an isolation transistor (T), a driving circuit (C and TR), and an organic light emitting diode (P), said driving circuit (C and TR) storing a value that determines the magnitude of the light emitted by that pixel (P), said driving circuit (C and TR) placing said OLED (P) in a conducting path between first (Column) and second (Row)

power terminals, said isolation transistor (T) connecting said driving circuit (C and TR) to a bit line (Column) when said isolation transistor (T) is placed in a conducting state by the application of a logic signal to a word line (Row) [figure 2; column 4, line 35 - column 5, line 45].

In regards to claim 2, Dingwall discloses said driving circuit (C and TR) comprises a storage capacitor (C) and a driving transistor (TR), said storage capacitor (C) storing a charge that determines the magnitude of the light emitted by said pixels (P), said driving transistor (TR) having a gate connected to said storage capacitor (C), said driving transistor (TR) connecting said OLED (P) between said first (Column) and second (Row) power terminals, said isolation transistor (T) connecting said storage capacitor (C) to said bit line (Column) when said isolation transistor (T) is placed in said conducting state by the application of said logic signal to said word line (Row) [figure 2; column 4, line 35 - column 5, line 45].

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall (5,903,246) in view of Hosokawa et al. (5,142,343).

In regards to claims 3 and 8, Dingwall discloses said OLEDs (P) are part of an array of OLEDs (P), said array comprising: a sheet (glass substrate) having first and second surfaces, said first and second surfaces being parallel to one another, said sheet being transparent to light of a first wavelength; a first electrode (ITO anode) comprising a first electrode layer in contact with said first surface, said first electrode layer being transparent to light of said first wavelength; a light emitting layer (organic hole transport layer) comprising an organic polymer in electrical contact with said first electrode layer; and a plurality of second electrodes (cathode), one such second electrode corresponding to each of said OLEDs (P), each of said second electrodes (cathode) comprising an isolated conducting area in contact with said light emitting layer, said light emitting layer generating light of said first wavelength in a region adjacent to said second electrode when a potential difference is applied across said first (anode) and second (cathode) electrodes [figure 1; column 3, line 42 - column 4, line 34]. Dingwall does not disclose expressly a flexible substrate.

However, Hosokawa et al. disclose a plastic substrate [column 4, Lines 35-39]. Dingwall and Hosokawa et al. are analogous art because they are from the field of organic light emitting diode display devices. At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Hosokawa's plastic substrate as Dingwall's substrate. The motivation for doing so would have been to save on manufacturing cost and weight. Therefore, it would have been obvious to combine Dingwall with Hosokawa et al. to obtain the invention as specified in claims 3 and 8.

6. Claims 4-7 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall (5,903,246) and Hosokawa et al. (5,142,343) as applied to claims 3 and 8 above, and further in view of Brown (5,184,114).

In regards to claims 4 and 9, Dingwall discloses said driving transistors (TR) are part of a transistor array (TR) having a plurality of connection points disposed on a surface, each of said connection points corresponding to one of said second electrodes (cathode) in said array of OLEDs (P), said connection points being arranged such that each second electrode (cathode) overlays said corresponding connection point when said array of OLEDs (P) is properly aligned with said transistor array (TR) [figure 1; column 3, line 42 - column 4, line 34]. Dingwall does not disclose expressly a bonding layer located between said transistor array (TR) and said array of OLEDs (P), said bonding layer electrically connecting each of said second electrodes (cathode) to that connection point corresponding to that second electrode (cathode).

However, Brown discloses a bonding layer electrically connecting each of said second electrodes (22) to a connection point corresponding to that second electrode (22). [figure 1; column 4, Lines 34-50]. Dingwall and Brown are analogous art because they are from the field of light emitting diode display devices. At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Brown's bonding layer in Dingwall's array. The motivation for doing so would have been to securely attach the transistor array to the array of OLEDs. Therefore, it would have been obvious to combine Dingwall with Brown to obtain the invention as specified in claims 4 and 9.

In regards to claims 5 and 10, Brown discloses said bonding layer comprises electrically conducting particles suspended in an electrically insulating adhesive [figure 1; column 4, Lines 34-50]. For the reasons set forth in the above rejection of claim 4, it would have been obvious to combine Dingwall with Brown to obtain the invention as specified in claims 5 and 10.

In regards to claims 6 and 11, Dingwall discloses a light conversion layer (color shutter) in contact with said second surface of said sheet (glass substrate), said light conversion layer (color shutter) absorbing light of said first wavelength and emitting light of a second wavelength [figure 1; column 4, lines 20-24].

In regards to claims 7 and 12, Dingwall discloses said driving transistors (TR) are part of an array of thin film transistors (TR) [column 1, lines 43-51].

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Turko et al. (5,121,214), Durand et al. (5,180,523), Gemma et al. (5,294,820), Norman et al. (5,424,560), Norman et al. (5,719,589), Huang et al. (5,789,766), Lebby et al. (5,818,404), Huang et al. (5,929,474) and Carey et al. (5,994,174) are cited to further show the state of the art with respect to displays comprising a plurality of light emitting diodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday from 6:30 AM to 3 PM E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on (703) 305-4938.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 308-9051, (for formal communications intended for entry)

**Or:**

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

VIJAY SHANKAR
PRIMARY EXAMINER

JP 12-29-99